What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having a memory formation region in which a memory device is formed and a logic formation region in which a logic device is formed;

a first impurity region formed in an upper surface of said semiconductor substrate in said memory formation region;

a second impurity region formed in the upper surface of said semiconductor substrate in said logic formation region;

a third impurity region formed in an upper surface of said first impurity region and having a conductivity type different from that of said first impurity region;

a fourth impurity region formed in an upper surface of said second impurity region and having a conductivity type different from that of said second impurity region;

a first silicide film formed in an upper surface of said third impurity region;

a capacitor formed above said first silicide film and electrically connected to said first silicide film; and

a second silicide film formed in an upper surface of said fourth impurity region and having a larger thickness than said first silicide film.

2. The semiconductor device according to claim 1, further comprising,

first and second gate structures formed on the upper surface of said semiconductor substrate in said memory formation region and spaced apart at a given distance from each other, and

third and fourth gate structures formed on the upper surface of said semiconductor substrate in said logic formation region and spaced apart at a given

distance from each other,

wherein said first and second silicide films are provided between said first and second gate structures and between said third and fourth gate structures, respectively, and

a first gate aspect ratio that is defined by the distance between said first and second gate structures and a height of said first and second gate structures is larger than a second gate aspect ratio that is defined by the distance between said third and fourth gate structures and a height of said third and fourth gate structures.

3. The semiconductor device according to claim 2, wherein said first gate aspect ratio is larger than 0.8.

4. The semiconductor device according to claim 1, further comprising,

a fifth impurity region formed in the upper surface of said semiconductor substrate in said logic formation region,

a sixth impurity region formed in an upper surface of said fifth impurity region and having a conductivity type different from that of said fifth impurity region, and

a third silicide film formed in an upper surface of said sixth impurity region and thinner than said second silicide film.

5. The semiconductor device according to claim 4, wherein each of said third, fourth and sixth impurity regions is a source/drain region of a MOS transistor.

6. The semiconductor device according to claim 4, further comprising,

first and second gate structures formed on the upper surface of said semiconductor substrate in said memory formation region and spaced apart at a given

distance from each other,

third and fourth gate structures formed on the upper surface of said semiconductor substrate in said logic formation region and spaced apart at a given distance from each other, and

fifth and sixth gate structures formed on the upper surface of said semiconductor substrate in said logic formation region and spaced apart at a given distance from each other,

wherein said first to third silicide films are provided between said first and second gate structures, between said third and fourth gate structures, and between said fifth and sixth gate structures, respectively, and

a first gate aspect ratio that is defined by the distance between said first and second gate structures and a height of said first and second gate structures and a third gate aspect ratio that is defined by the distance between said fifth and sixth gate structures and a height of said fifth and sixth gate structures are both larger than a second gate aspect ratio that is defined by the distance between said third and fourth gate structures and a height of said third and fourth gate structures.

7. The semiconductor device according to claim 6, wherein said first and third gate aspect ratios are each larger than 0.8.

8. The semiconductor device according to claim 6, further comprising:

an interlayer insulating film formed over said semiconductor substrate and covering said first to sixth gate structures;

a first contact plug provided in and through said interlayer insulating film and connected to said third silicide film;

an insulating layer provided on said interlayer insulating film; and

a second contact plug provided in and through said insulating layer and connected to said first contact plug,

wherein said capacitor is provided in said insulating layer.

9. A semiconductor device manufacturing method, comprising the steps of:

(a) preparing a semiconductor substrate having a memory formation region where a memory device is to be formed and a logic formation region where a logic device is to be formed;

(b) forming first and second impurity regions in an upper surface of said semiconductor substrate in said memory formation region and said logic formation region, respectively;

(c) forming first and second gate structures spaced apart at a given distance from each other on the upper surface of said semiconductor substrate in said memory formation region, and forming a third impurity region in an upper surface of said first impurity region between said first and second gate structures, said third impurity region having a conductivity type different from that of said first impurity region;

(d) forming third and fourth gate structures spaced apart at a given distance from each other on the upper surface of said semiconductor substrate in said logic formation region, and forming a fourth impurity region in an upper surface of said second impurity region between said third and fourth gate structures, said fourth impurity region having a different conductivity type from said second impurity region;

(e) applying a nondirectional sputtering method from above the structure obtained by said steps (c) and (d) to deposit a metal material on said third impurity region between said first and second gate structures and on said fourth impurity region between

said third and fourth gate structures;

(f) causing said metal material and said semiconductor substrate to react with each other to form silicide films in the upper surfaces of said third and fourth impurity regions; and

(g) forming a capacitor above said silicide film in the upper surface of said third impurity region, said capacitor being electrically connected to said silicide film in the upper surface of said third impurity region;

a first gate aspect ratio that is defined by the distance between said first and second gate structures and a height of said first and second gate structures being larger than a second gate aspect ratio that is defined by the distance between said third and fourth gate structures and a height of said third and fourth gate structures.

10. The semiconductor device manufacturing method according to claim 9, wherein said first gate aspect ratio is larger than 0.8.

11. The semiconductor device manufacturing method according to claim 9,

wherein in said step (b), a fifth impurity region is further formed in the upper surface of said semiconductor substrate in said logic formation region,

said semiconductor device manufacturing method further comprises the step (h) of, prior to said step (e), forming fifth and sixth gate structures spaced apart at a given distance from each other on the upper surface of said semiconductor substrate in said logic formation region and forming a sixth impurity region in an upper surface of said fifth impurity region between said fifth and sixth gate structures, said sixth impurity region having a conductivity type different from that of said fifth impurity region,

in said step (e), said nondirectional sputtering method is applied from above the

structure obtained through said steps (c), (d), and (h) so as to deposit said metal material also on said sixth impurity region between said fifth and sixth gate structures,

in said step (f), said metal material and said semiconductor substrate are caused to react with each other to further form said silicide film also in the upper surface of said sixth impurity region, and

said second gate aspect ratio is smaller than a third gate aspect ratio that is defined by the distance between said fifth and sixth gate structures and a height of said fifth and sixth gate structures.

12. The semiconductor device manufacturing method according to claim 11, wherein each of said third, fourth and sixth impurity regions is a source/drain region of a MOS transistor.

13. The semiconductor device manufacturing method according to claim 11, wherein said first and third gate aspect ratios are each larger than 0.8.

14. The semiconductor device manufacturing method according to claim 11, further comprising the steps of:

(i) between said step (f) and said step (g), forming an interlayer insulating film over said semiconductor substrate, said interlayer insulating film covering said first to sixth gate structures;

(j) before said step (g), forming a first contact plug in and through said interlayer insulating film, said first contact plug being connected to said silicide film formed in the upper surface of said sixth impurity region;

said step (g) forming an insulating layer on said interlayer insulating film and

forming said capacitor in said insulating layer; and

(k) forming a second contact plug in and through said insulating layer, said second contact plug being connected to said first contact plug.